HP 64785A Emulator for Hitachi SH7032 and 7034 Microprocessors

Product Overview

Design, debug, and integrate real-time embedded systems

The HP 64785A active probe emulator supports Hitachi SH7032 and SH7034 microprocessors up to 20 MHz.* This emulator supports SH7032/34 processors in 5-V versions. The system offers the real-time measurement capabilities needed to develop SH7032/34 embedded systems, including interpreted displays of on-chip registers, emulation memory, a deep-trace analyzer, and hardware break events.

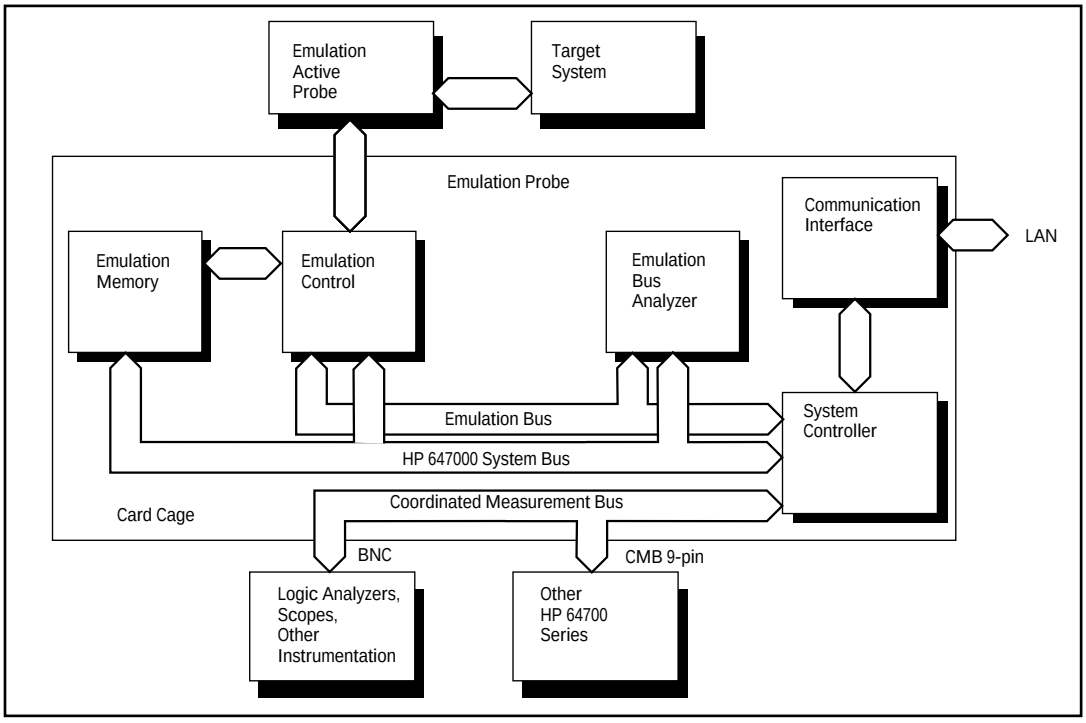
HP's host-independent emulation and analysis systems can be controlled from a simple terminal, HP 9000 workstations, or Sun SPARCstations. Access to these systems is through a selection of user interfaces, including an X/Motif-based embedded debug environment for HP workstations and Sun SPARCstations. This allows you to open several emulation and analysis windows for simultaneous display during a session, providing visibility on several parameters at once.

Features

- No-wait state execution up to 20 MHz*
- Support for SH7032 and 7034 processors
- Configuration menu for easy emulator setup
- Display and modify functions for internal I/O registers
- Background monitor
- Eight real-time hardware break events
- Unlimited software execution breakpoints
- Support for the fast file download
- Termination to a 112-pin QFP package
- Three-foot probe cable terminating in an active probe
- Flexible probing to target system by 9-inch QFP flexible cable
- QFP socket adapter, soldered on target system, for both the emulator probe and a QFP real chip
- Memory for internal RAM/ROM and monitor support configurations without an optional emulation memory module for a single chip application
- Simulated I/O (on workstation)
- Cross-triggering between another emulator, logic analyzer, or oscilloscope
- Support for Hitachi compiler and assembler on HP 9000/700 and Sun SPARCstations
- Support for Green Hills Software, Inc. compiler and assembler on HP 9000/700, Sun SPARCstations, and IBM PC compatibles

* Contact your HP 64000 field engineer for the latest configuration information and supported processor speeds.

Modular HP 64700 Series system



HP 64700 Series development tools include emulators and emulation bus analyzers.

Emulation Bus Analyzer

- 80 channels available with trace buffer depths of 1 K, 8 K, 64 K, or 256 K
- Postprocessed software-based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators that can be sequenced up to 8 levels deep
- Time tag with 20-ns resolution (64794x) and state counts
- Prestore capability

Emulation Memory

- One-state access up to 20 MHz (HP 64172A/B)
- One-state access up to 16.6MHz and two-state access above 16.6 MHz (HP 64173A/B)
- Display and modification of emulation memory with minimum processor interruption by the quick break of background monitor
- 256-KB, 1-MB and 4-MB memory configurations
- Mapping resolution of 16-KB for 64172A, 32 KB for 64172B, and 128 KB for 64173A

Software Support

- Real-time operating system measurement tools

Card Cage

The card cage is the basis for modular emulators and analyzers. It can be disassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The card cage host control card contains LAN capability, along with RS-232-C/RS-422 serial port and system configuration firmware. System, emulation, and analysis firmware are always resident and may be updated.

Networking

In many embedded design environments, it is not possible for each member of a design team to have a target system and an emulator, which makes remote access from a networked host essential. The HP 64700 Series emulators offer a LAN connection so that you can share a central emulator and target from either a PC or a workstation.

In addition, the rapid file transfers—rates of up to 6 MB per minute—increase your productivity. The card cage connects to all popular Ethernet/803.2 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI (attachment unit interface). The system supports TCP/IP protocols, LAN gateways, and ARPA/Berkeley standards.

Emulation Bus Analysis
Emulation bus analysis provides real-time, nonintrusive operation along with extensive triggering, tracing, and qualification features. Analysis features include selective tracing, time-tagging, prestore, and a selection of 1-K, 8-K, 64-K, or 256-K trace depths . These comprehensive resources combine to help you solve both simple and complex problems.

The dual-bus architecture results in real-time, nonintrusive analysis. You can set up and review traces without breaking processor execution. Selective tracing of microprocessor code flow without breaking execution is a major strength of the HP 64700 Series emulators and analyzers.

You can combine up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, in sequential trace specifications using “find A, followed by B...” constructs up to eight levels deep. Apply a range comparator to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent executions or store only specified execution information.

Precise time-tagging of events helps you identify discrepancies in code execution. The analyzer logs each event with its execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore helps you pinpoint possible problem areas in your code, by determining which of several different functions is accessing a variable and is responsible for corrupting it.

Real-Time Emulation
The HP 64785A contains the microprocessor, emulation monitor, run-control circuits, and up to 4 MB emulation memory. This emulator includes a background monitor, which uses no target address space. The background monitor can display and modify emulation memory with minimum processor interruption by the quick break, typically 200 or 300 µs.

HP high-speed emulation memory provides you with no-wait state real- time execution, one-state memory access, which is a significant feature of SH7032 and 7034 microprocessors. HP 64172A 256-KB and HP 64172B 1-MB emulation memory support one-state-access up to the maximum speed, 20 MHz. HP 64173A 4-MB emulation memory supports it up to 16.6 MHz and two-state access above 16.6 MHz.

Extensive breakpoint capabilities are included, allowing you to define where to stop code execution. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point.

Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at a processor address, data, status points, or a combination of all three.

Flexible Memory Configuration
Memory modules provide emulation memory. One slot is available on the active probe, allowing you to plug in the amount of memory you need up to 4 MB. If you initially order less than the maximum amount, you can easily expand by replacing it with the appropriate module. Modules for 256 KB (HP 64172A), 1 MB (HP 64172B), and 4 MB (HP 64173A) are available.

Symbolic Support
Symbolic debugging clarifies trace-list interpretation by allowing you to see program symbols in the trace list.This feature facilitates quick identification of problems involving the interaction of software and hardware. You can also use symbols in emulation commands and expressions to simplify command entries and user interaction.

Workstation-Hosted Environment
The HP embedded debug environment is an emulator/analyzer user interface for software development.

The emulator/analyzer tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level microprocessor run control.

The HP debug environment supports language tools from Hitachi and Green Hills Software, Inc., which provide software tools compatible with the HP 64785A emulator. Both toolsets include C cross-compiler and an assembler.

Terminal Mode Operation
A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; the system accepts file transfers using industry-standard formats. Because a terminal can access these commands, host independence is realized.

HP 64785A Emulator Specifications

Processor Compatibility

Model HP 64785A:
Hitachi SH7032/34 in 5 V version

Electrical

Maximum Clock Speed:	20 MHz* with no-wait states required for emulation or target system memory.

*HP 64172A/B emulation memory supports one-state access up to 20 MHz. HP 64173A emulation memory supports one-state access up to 16.6 MHz and two-state access above 16.6 MHz

Minimum Clock Speed:	2MHz
Power:	Primary power supplied by card cage

Environmental

Temperature:	Operating, 0 to +40 °C (+32 to +104 °F) Non-operating, -40 to +60 °C (-40 to 140 °F)
Altitude:	Operating, 4600 m (15,000 ft) Non-operating, 15300 m (50,000 ft)

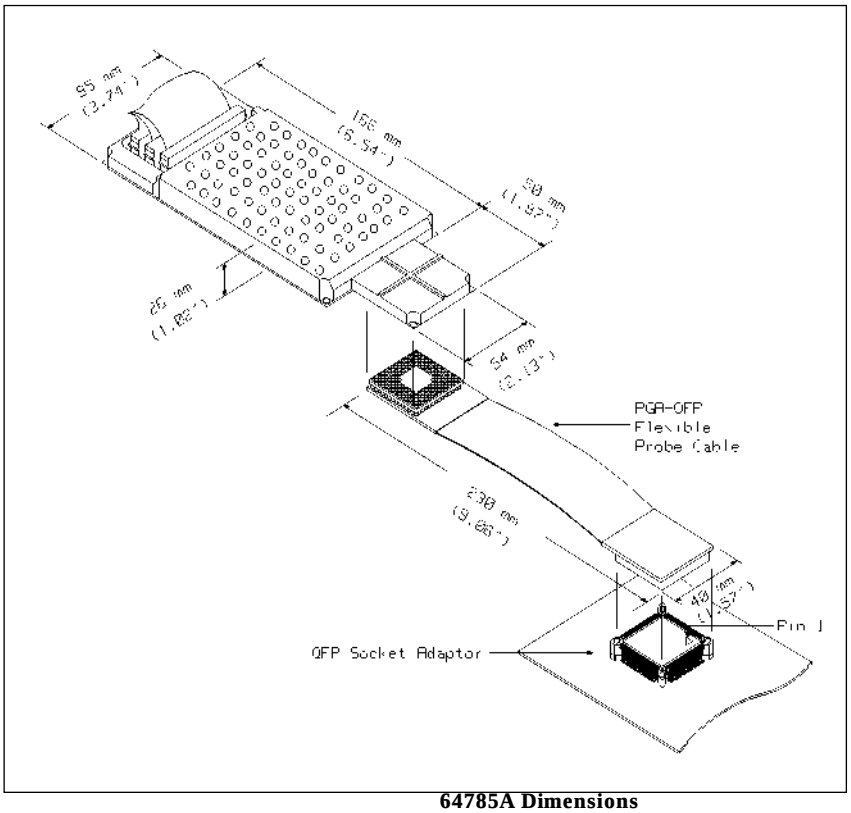
Regulatory Compliance
when installed in HP 64700 card cage

Electromagnetic A Interference:	EN55011 Group1 Class
Safety:	Self-certified to UL 1244, IEC 348, CSA-231

Physical

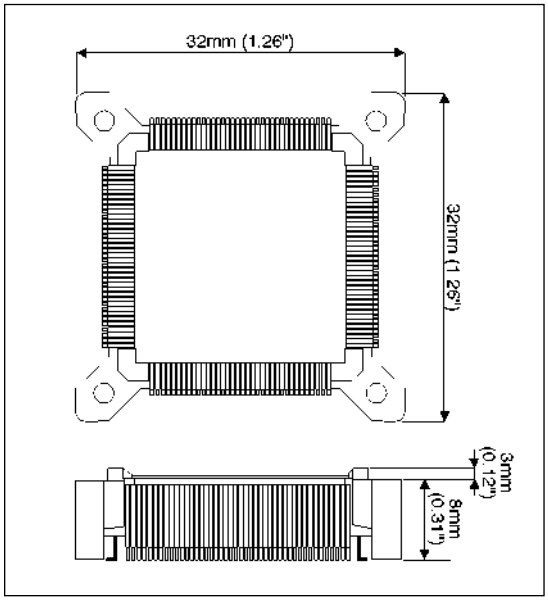
Cable length:	Probe to card cage approximately 1 m (40")

Dimensions: see drawings at right



64785A Dimensions

Notice for the QFP Socket Adapter
The QFP socket adapter is an expendable supply because the electrical contacts degrade gradually as the flexible probe cable is attached and detached. One QFP socket adapter is supplied with HP 64785A. Please prepare some spares of the QFP socket adapter in advance. The part number is HP 64784-61611.



QFP Socket Adapter Dimensions

HP 64785A AC Timing Specifications: 20MHz

Characteristic	Symbol	SH7034 20 MHz		HP 64785A Worst Case		Typical
		Min	Max	Min	Max	(*1)
EXTAL input high-level pulse	tEXH	10 ns				10 ns
EXTAL input low-level pulse	tEXL	10 ns				10 ns
EXTAL input rise time	tEXr		5 ns			5 ns
EXTAL input fall time	tEXf		5 ns			5 ns
Clock cycle time	tcyc	50 ns	500 ns			50,500 ns
Clock high-pulse width	tCH	20 ns				24 ns
Clock low-pulse width	tCL	20 ns				18 ns
Clock rise time	tCr		5 ns			4 ns
Clock fall time	tCf		5 ns			4 ns
Reset oscillation setting time	tOSC1	10 ms		10 ms		10 ms
Software standby oscillation setting time	tOSC2	10 ms		10 ms		10 ms
RESET setup time	tRESS	200 ns		250 ns		
RESET pulse width	tRESW	20 t cyc			20 t cyc	
NMI reset setup time	tNMIRS	200 ns		235 ns		
NMI reset hold time	tNMIRH	200 ns		200 ns		
NMI setup time	tNMIS	100 ns		110 ns		
NMI hold time	tNMIH	50ns		50 ns		
IRQ0-IRQ7 setup time (edge detection time)	tIRQES	100 ns		110 ns		
IRQ0-IRQ7 setup time (level detection time)	tIRQLS	100 ns		110ns		
IRQ0-IRQ7 hold time	tIRQEH	50 ns		50 ns		
IRQOUT output delay time	tIRQOD		50 ns		50 ns	
Bus request setup time	tBRQS	50ns		55 ns		
Bus acknowledge delay time 1	tBACD1		50 ns		55 ns	
Bus acknowledge delay time 2	tBACD2		50 ns		55 ns	
Bus 3-state delay time	tBZD		50 ns		55 ns	
Address delay time	tAD		20 ns		30 ns	13 ns
CS delay time 1	tCSD1		25 ns		30 ns	10 ns
CS delay time 2	tCSD2		25 ns		30 ns	6 ns
CS delay time 3	tCSD3		20 ns		25 ns	9 ns
CS delay time 4	tCSD4		20 ns		25 ns	5 ns
Access time 1 from read strobe (35% duty)	tRDAC1	12.5 ns		2.5 ns		12.5 ns
Access time 1 from read strobe (50% duty)	tRDAC1	5 ns		-5 ns		5 ns
Access time 2 from read strobe (35% duty)	tRDAC2	62.5 ns		52.5ns		62.5 ns
Access time 2 from read strobe (50% duty)	tRDAC2	55 ns		45 ns		55 ns
Read strobe delay time	tRSD		20 ns		25 ns	8 ns
Read data setup time	tRDS	15 ns		25 ns		15 ns
Read data hold time	tRDH	0ns		0ns		0 ns
Write strobe delay time 1	tWSD1		20 ns		25 ns	10 ns
Write strobe delay time 2	tWSD2		20 ns		25 ns	6ns
Write strobe delay time 3	tWSD3		20 ns		25 ns	11ns
Write strobe delay time 4	tWSD4		20 ns		25 ns	8 ns
Write data delay time 1	tWDD1		35 ns		40 ns	21 ns
Write data delay time 2	tWDD2		20 ns		40ns	23 ns
Write data hold time	tWDH	0 ns		-5 ns		2 ns

Characteristic	Symbol	SH7034 20 MHz		HP 64785A Worst Case		Typical
		Min	Max	Min	Max	(*1)
Parity output delay time 1	tWPDD1		40 ns		45 ns	24 ns
Parity output delay time 2	tWPDD2		20 ns		25 ns	11 ns
Parity output hold time	tWPDH	0 ns		-5 ns		3 ns
Wait setup time	tWTS	14 ns		24 ns		10 ns
Wait hold time	tWTH	10 ns		10 ns		10 ns
Read data access time 1	tACC1	20 ns		5 ns		20 ns
Read data access time 2	tACC2	70ns		55ns		70ns
RAS delay time 1	tRASD1		20ns		25ns	8ns
RAS delay time 2	tRASD2		30ns		35ns	14ns
CAS delay time 1	tCASD1		20ns		25ns	6ns
CAS delay time 2	tCASD2		20ns		25ns	9ns
CAS delay time 3	tRASD3		20ns		25ns	8ns
Column address setup time	tCAC1	0ns		-5ns		13ns
CAS to read data access time 1 (35% duty)	tCAC1	13.5ns		3.5ns		13.5ns
CAS to read data access time 1 (50% duty)	tCAC1	6ns		-4ns		6ns
CAS to read data access time 2	tCAC2	25 ns		15 ns		25 ns
RAS to read data access time 1	tRAC1	55 ns		45 ns		55 ns
RAS to read data access time 2	tRAC2	105 ns		95 ns		105 ns
High-speed page mode CAS precharge time 1	tCP	12.5 ns				24 ns
AH delay time 1	tAHD1		20 ns		25 ns	6 ns
AH delay time 2	tAHD2		20 ns		25 ns	8 ns
Multiplexed address delay time	tMAD		30 ns		35 ns	16 ns
Multiplexed address hold time	tMAH	0 ns		-5 ns		6 ns
DACK0-DACK1 delay time 1	tDACD1		23 ns		28ns	
DACK0-DACK1 delay time 2	tDACD2		23 ns		28 ns	
DACK0-DACK1 delay time 3	tDACD3		20 ns		25 ns	
DACK0-DACK1 delay time 4	tDACD4		20 ns		25 ns	
DACK0-DACK1 delay time 5	tDACD5		20 ns		25 ns	
Read delay time (35% duty) 27 ns	tRDD		29.5 ns		34.5 ns	
Read delay time (50% duty)	tRDD		40 ns		45ns	35ns
Data setup time for CAS	tDS	0 ns		-5 ns		6 ns
CAS setup time for RAS	tCSR	10 ns		5 ns		19 ns
Row address setup time	tRAH	10 ns		5 ns		20 ns
Write command hold time	tWCH	15 ns		10 ns		31 ns
Write command setup time (35% duty)	tWCS	0 ns		-5 ns		7 ns
Write command setup time (50% duty)	tWCS	0 ns		-5 ns		14 ns

*1 Typical outputs measured with 50 pF load

Ordering Information

Terminal-Based Emulation System for SH7032/34 Processor	
Model	**Description**
64785A	20-MHz active probe emulator with space for up to 4 MB of emulation memory for SH7032/34 processors (includes demo board, 112-pin QFP flexible cable, and QFP socket adapter)
64748C	Emulation control card
64794A	8K-deep emulation bus analyzer card, 80 channels
64700B	Card cage

Emulation System Options	
Model	**Description**
64172A	256 KB, SRAM memory module (20 ns)
64172B	1 MB, SRAM memory module (20 ns)
64173A	4 MB, SRAM memory module (25 ns)
64704A	1 K-deep 80-channel emulation bus analyzer card
64794C	64 K-deep emulation bus analyzer card, 80 channels
64794D	256 K-deep emulation bus analyzer card, 80 channels
64023A	CMB cable (4 m; includes three 9-pin connectors)

Software Options

For each software model number ordered, purchase one media option and at least one license option for each concurrent user:

Model	Description
B3076B	Graphical user interface

Media/License Options	
opt AAH	HP 9000 Series 300/400 manuals/media (DDS DAT tape)
opt AAX	HP 9000 Series 300/400 manuals/media (1/4 inch cartridge tape)
opt UBX	HP 9000 Series 300/400 single-user license
opt AAY	HP 9000 Series 700 manuals/media (DDS DAT tape)
opt UBY	HP 9000 Series 700 single-user license
opt AAV	Sun SPARCstation manuals/media (1/4 inch cartridge tape)
opt UBV	Sun SPARCstation single-user license

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

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